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MARLBOROUGH, MA OFFICE  
TELEPHONE (508) 485-7772

MAILING ADDRESS:  
P.O. BOX 9169  
BOSTON, MA 02209

101 FEDERAL STREET  
BOSTON, MA 02110  
(617) 439-4444  
FAX (617) 439-4170

DIKE, BRONSTEIN, ROBERTS & CUSHMAN  
*Intellectual Property Practice Group*

WASHINGTON, DC  
TELEPHONE (703) 553-2563

## FACSIMILE TRANSMITTAL

**DATE:** January 28, 2004

**TO:** U.S. Patent & Trademark Office  
Examining Group 2800

**FAX NO.:** 1-703-872-9318

**FROM:** Steven M. Jensen

**FAX NO.:** 617-439-4170

**Our Docket No.:** 56386 (71987)

**No. of Pages (incl. cover):** 5

**Re:** U.S. Serial Number 09/932,053

**MESSAGE:**

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Docket No. 56386 (71987)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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JAN 28 2004

APPLICANT: C. Wu et al.

U.S.S.N.: 09/932,053

GROUP: 2823

FILED: August 18, 2001

EXAMINER: H. Lee

OFFICIAL

FOR: SEMICONDUCTOR PACKAGE AND FABRICATING METHOD  
THEREOF

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted by facsimile to Group 2800 of the U.S. Patent & Trademark Office by facsimile number 703-872-9318 on January 28, 2004.

By:

Steven M. Jensen

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

RESPONSE TO OFFICE ACTION

Applicants are in receipt of the Office Action dated October 28, 2003 of the above-referenced application. Applicants respond to the Office Action as follows.

Applicants' claimed invention is directed to a semiconductor package and fabricating method in which a semiconductor chip is positioned above a plurality of passive devices, so as to reduce the space occupied on a substrate. As shown in FIGS. 4C and 4D, the passive devices 3 are mounted on the substrate 2 and encapsulated by an insulative material 4 before a semiconductor chip 5 is stacked on the insulative material 4. As a result, the chip 5 is situated above the passive devices 3 without contacting the substrate. Subsequently, the chip 5 and bonding wires 6 are encapsulated by an encapsulant 7 (see FIG. 4E).

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The above-described semiconductor package and fabricating method can yield significant benefits. Due to the vertical arrangement of the semiconductor chip and the passive devices, a reduced area of the substrate is occupied (see specification at page 4, lines 13-15), as compared to prior art packages in which passive devices are positioned beside a semiconductor chip. Moreover, the passive devices are encapsulated by the insulative material before mounting of the semiconductor chip, thereby preventing direct contact between the passive devices and bonding wires, and eliminating the occurrence of short circuits (see specification at page 4, line 24 to page 5, line 2).

Claims 1-5, 7, 10-15, 17, and 20 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 5,355,283 to Marrs et al. (hereinafter "Marrs") in view of U.S. Patent 5,249,354 to Richman (hereinafter "Richman"). Claims 6, 8, 9, 16, 18, and 19 were rejected under 35 USC 103(a) as being unpatentable over "Marrs and Richman ... and further in view of" U.S. Patent 6,022,583 to Falcone et al. (hereinafter "Falcone"). These rejections are respectfully traversed, for reasons discussed in the Amendment dated July 14, 2003, and for the additional reasons provided below.

In the Amendment dated July 14, 2003, Applicants included the following remarks:

Marrs explicitly states that "[p]assive components, such as resistors and capacitors, can also be mounted on the substrate" (column 2, lines 66-67). In other words, passive components optionally are included in the package of Marrs, and would be mounted on the substrate. However, Marrs does not teach or suggest that the semiconductor chip would be disposed above the passive components and free of contact with the passive components and the substrate, as required in claims 1 and 11 of the Applicants' invention. (Amendment, Page 4, emphasis in original)

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On page 5 of the Office Action dated October 28, 2003, the Examiner stated:

After mounting the passive components on the substrate, the insulating material 609 is covered on the substrate 602 followed by mounting the semiconductor chip 601 thereon. In other words, Marrs et al. teach that the insulating material 609 (i.e. the protruding portion of the insulating material 609 over a central region of the substrate 602) physically separates the semiconductor chip 601 from the passive components and the substrate 602. Thus, the semiconductor chip 601 does not contact with the passive devices and the substrate. (emphasis in original)

Applicants respectfully traverse these allegations. Marrs simply does not teach or suggest that the insulating material 609 physically separates the semiconductor chip 601 from the passive components and the substrate 602. No passage in Marrs has been cited to support this statement, and indeed none exists in the Marrs reference. With reference to FIG. 6 of Marrs, it is clear that the cited "insulating material" is actually an epoxy resin 609 that fills vias 607 in the substrate 602 (see also column 7, lines 13-16). Therefore, in Marrs, the epoxy resin 609 is filled in vias 607 inside the substrate 602 (column 7, line 12).

On page 5 of the Office Action, as reproduced above, the following statement was used to describe the epoxy resin 609: "(i.e. the protruding portion of the insulating material 609 over a central region of the substrate 602)..." It is not clear what constitutes a "protruding portion" in Marrs, and regardless, no protruding portion is required by the claims. The Examiner has not identified any "insulative material" in Marrs for encapsulating the passive devices, as required in claims 1 and 11.

Marrs also does not teach or suggest pre-encapsulating a passive device with insulating material before mounting the semiconductor chip **above** the passive device. In particular, Marrs does not teach or suggest "disposing a semiconductor device on a surface of the insulative material above the passive devices..." (claim 1), or "a semiconductor chip disposed on a surface of the insulative materials above the passive devices..." (claim 11).

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As discussed in the Amendment dated July 14, 2003, Marrs does not teach or suggest an arrangement in which the semiconductor chip is free of contact with the passive devices and the substrate, as recited in claims 1 and 11.

Richman fails to remedy the deficiencies of the Marrs reference. Richman was cited for disclosing a plurality of bonding wires for electrically connecting a chip to bonding fingers. However, even if Richman were somehow combined with Marrs, the combination still fails to teach or suggest a semiconductor package or fabricating method in which a semiconductor chip is positioned above pre-encapsulated passive devices and free of contact with the passive components and a substrate, as required in claims 1 and 11 of the Applicants' invention. Instead, Richman teaches enclosing the chip and/or other active or passive components in an encapsulation layer. Therefore, claims 1 and 11 and the respective dependent claims are patentable over the combination of Marrs in view of Richman.

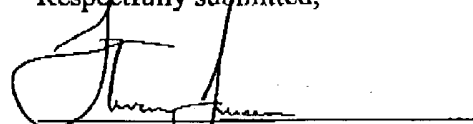
Regarding the rejection of claims 6, 8, 9, 16, 18, and 19 as being unpatentable over Marrs in view of Richman, and further in view of Falcone, the Falcone reference discloses a method of dispensing encapsulant material on a wire-bonded die. However, Falcone fails to teach or suggest pre-encapsulating a passive device with insulative material before mounting the semiconductor chip on the insulative material. Therefore, Falcone cannot be combined with the Marrs and Richman to produce the Applicants' invention as recited in the above claims.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

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Phone: (617) 439-4444  
Customer No. 21874

Respectfully submitted,



Peter F. Conless (Reg. No. 33,860)  
Steven M. Jensen (Reg. No. 42,693)  
Dike Bronstein, Roberts & Cushman  
Intellectual Property Practice Group  
EDWARDS & ANGELL, LLP  
P.O. Box 9169  
Boston, MA 02209